REMARKS/ARGUMENTS

Claims 15, 27, 35-39 and 41 are in the application, of which claims 15, 27 and 37 are the independent claims. Claims 15, 27 and 37 are amended herein. Claims 1-14, 16-26, 28-34 and 40 have been previously canceled. No claims are added or canceled herein. No new matter is believed to have been introduced to the application by this paper. Reconsideration and further examination are respectfully requested.

Claim Rejections – 35 USC §112

Claims 15, 27, 35-39 and 41 are rejected under 35 U.S.C. §112, second paragraph as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Office Action asserts that the limitation in claims 15, 27, and 37 of "...and prior to wafer testing of said semiconductor wafer..." is vague and ambiguous in that it is not clear whether a wafer testing step is a required limitation.

Claims 15, 27, and 37 have been amended to remove the phrase ""and prior to wafer testing of said semiconductor wafer." Accordingly, reconsideration and withdrawal of this rejection of independent claims 15, 27, and 37 and their dependent claims 35-36, 38-39, and 41 are respectfully requested.

Claim Rejections – 35 USC §103

Claims 15 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kajiwara et al. (U.S. Publication 2003/0127747, hereinafter "Kajiwara") in view of Hikita et al. (U.S. Publication 2003/0146518, hereinafter "Hikita") and Broz et al. (U.S. Publication 2004/0115934, hereinafter "Broz"). **Claims 35** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara in view of Hikita and Broz, as applied to claim 15, and further in view of Dass et al. (U.S. Patent 6,162,652, hereinafter "Dass"). **Claims 27 and 37-38** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara in view of Fan et al. (U.S. Patent 6,956,292, hereinafter "Fan"), Hikita, and Broz. **Claims 36 and 41** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara in view of Fan, Hikita, and Broz, as applied to claims 27 and

37 above, and further in view of Dass. **Claim 39** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara in view of Fan, Hikita, and Broz, as applied to claim 37 above, and further in view of Zhang et al. (U.S. Patent 6,104,461, hereinafter "Zhang"). Reconsideration and withdrawal of these rejections are respectfully requested.

Amended claim 15 is drawn to a method for fabricating a circuit component. The method includes the step of providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening. The method also includes the step of providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured for a package interconnect, wherein said metal bump has a substantially vertical exposed sidewall extending from a bottom of said metal bump to a substantially planar exposed top surface of said metal bump. The method further includes the step of, after said providing said exposed metallization structure, performing a sputter etching process with an argon gas.

Amended claim 27 is drawn to a method for fabricating a circuit component. The method includes the step of providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer over said semiconductor wafer and on said second region, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening. The method also includes the step of providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured for a package interconnect, wherein said metal bump has a substantially vertical exposed sidewall extending from a bottom of said metal bump to a substantially planar exposed top surface of said metal bump. The method also includes the

step of, after said providing said exposed metallization structure, performing an ion milling process with an argon gas.

Amended claim 37 is drawn to method for fabricating a circuit component. The method includes the step of providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening. The method also includes the step of providing an exposed metallization structure directly on said passivation layer, on said first region and over said semiconductor wafer, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured for a package interconnect, wherein said metal bump has a substantially vertical exposed sidewall extending from a bottom of said metal bump to a substantially planar exposed top surface of said metal bump. The method also includes the step of, after said providing said exposed metallization structure, performing an ion milling process with an inert gas.

The applied references are not seen to disclose or suggest the foregoing features of each of independent claims 15, 27 and 37.

In this regard, Broz is seen to teach that "*In the prior art, the integrated circuit is essentially in its finished state at this point. However, the pad surface is covered with metal fluorides, metal oxides, organic residues, and contaminants resulting from the protective overcoat etch, as well as from the photoresist ash. The residues and contaminants can have an adverse effect on the contact resistance of the pad. The wafer may be sintered and then baked. FIG. 1d illustrates the contact between a test probe 110 and the pad 102, while FIG. 1e shows a ball bond 111 of a gold wire 112 to the pad 102, and FIG. 1f shows a redistribution trace 114 as is used in Bond Over Active Circuitry (BOAC) metallization schemes. <u>In all of these applications</u>, removal of pad contaminants is an important part of achieving lower contact resistance.*" Broz, para. [0016], [*emphasis added*]. Based on the above disclosure, Bonz's step of removal of pad contaminants is seen to be performed <u>prior</u> to establishing contact between test

probe 110 and pad 102, prior to forming ball bond 111 of gold wire 112, and prior to forming redistribution trace 114.

Even if, *in arguendo*, Broz's process is combined with Kajiwara's device, this would result in Bonz's step of removal of pad contaminants being performed to clean Kijiwara's Al electrode pad 4 before Kijiwara's Au bump 7 is formed. Furthermore, such a combination would suggest that Broz's test probe 110 would be considered to contact Kijiwara's Al electrode pad 4 before Kijiwara's Au bump 7 can be formed on Kijiwara's Al electrode pad 4. However, Broz's test probe 110 would not be considered to contact Kijiwara's Au bump 7 because Broz's test probe 110 is not taught to contact any metal bump. Accordingly, Kajiwara and Broz, alone or combined, are not seen to disclose the claimed subject matter that "*after said providing said exposed metallization structure, performing a sputter etching process with an argon gas*" recited in claim 15 or "*performing an ion milling process with an argon gas*" as recited in claims 27 and 37, wherein each claim earlier recites "*said exposed metallization structure comprises a metal bump.*" Hikita is not seen to cure this deficiency as Hikita teaches a method for fabricating metal bumps and various shapes of bumps. With respect to claims 27 and 37, Fan are not seen to cure this deficiency as Fan also teaches a method of forming a metal bump. Therefore, claims 15, 27, and 37 are seen to patentable over the cited references and reconsideration and withdrawal of the rejections of claims 15, 27, and 37 are respectfully requested.

The other claims currently under consideration in the application are dependent from the independent claims discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested.

The absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the arguments made above may not be exhaustive, there may be other reasons for patentability of any or all claims that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper,

and the amendment or cancellation of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment or cancellation.

CONCLUSION

In view of the Amendments and Remarks herein, Applicants submit that the claims are in condition for allowance and respectfully request a notice to this effect. Should the Examiner have any questions, please call the undersigned at the phone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,
McDERMOTT WILL & EMERY LLP

/Dennis A. Duchene/
Dennis A. Duchene
Registration No. 40,595

11682 El Camino Real, Suite 400
San Diego, CA 92130
Phone: 858.720.3300 DAD/GR:nsn
Facsimile: 858.720.7800
Date: February 2, 2011

Please recognize our Customer No. 89518 as our correspondence address.